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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,271	08/22/2006	Shunpei Yamazaki	0756-7804	6014

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EXAMINER	
JAHAN, BILKIS	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,271	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/7/10 has been entered.

Claim Objections

Claim 1 is objected to because of the following informalities:

Claim 1 recites "…..the light emitting element has a layer for conducting photoelectric conversion…." However the light emitting element does not function conducting photoelectric conversion.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious

at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonezawa et al (Yonezawa, US 2003/0032213 A1) in view of Kimura (US 2003/0052324) A1.

Regarding claim 1, Yonezawa discloses a semiconductor device (Figures 2C, 21, 23B, 25C) comprising:

- an antenna 2708 (Fig. 25C, Para. 318), an integrated circuit 421 (Fig. 23B, Para. 289) comprising a thin film transistor 421 (Fig. 23B, Para. 289), a light-emitting element 433 (Fig. 23B, Para. 293), and
- the light receiving element 441 has a layer for conducting photoelectric conversion using a non-single crystal thin film (Para. 243),
- wherein the integrated circuit 421 includes a power supply circuit (Fig. 21, element Vi) configured to generate a power supply voltage (Para. 233) by using an alternating voltage generated by the antenna 2708, and
- wherein the antenna 2708, the light-emitting element 433 and the light-receiving element 441 (Fig. 23B, Para. 287) are electrically connected to the integrated circuit 421 on the same substrate 2702 (Fig. 25C, Para. 318)

- Yonezawa does not explicitly disclose the light emitting element 6050 has a layer for conducting photoelectric conversion using a non-single crystal thin film;
- However, Kimura discloses the light emitting element 6050 (Fig. 10B, Para. 169) has a layer 5007, 5008, 5045 (Fig. 5A, Fig. 6C, Para. 125, Para. 146) for conducting photoelectric conversion using a non-single crystal thin film (Para. 125, Para. 146). The above modification is used to control the photo electric conversion elements (Para. 4) and photo electric conversion elements can attain sufficient signal amplitude and reduce cost of the device (Para. 29). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Yonezawa's structure with Kimura's structure as suggested above to control the photo electric conversion elements (Para. 4) and photo electric conversion elements can attain sufficient signal amplitude and reduce cost of the device (Para. 29).

Regarding claim 2, Yonezawa in view of Kimura discloses limitations in claim 1 above and Yonezawa further discloses the integrated circuit 421, the light-emitting element 433 and the light-receiving element 441 are formed on the same substrate 2702.

Regarding claim 3, Yonezawa in view of Kimura discloses limitations in claim 1 above and Yonezawa further discloses the antenna 2708, the integrated circuit 421, the

light-emitting dement 433 and the light-receiving element 441 are formed on the same substrate 2702.

Regarding claims 10, 11, Yonezawa in view of Kimura discloses all limitations in claims 1, 2 above.

Claims 5-7, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonezawa et al (Yonezawa, US 2003/0032213 A1), Kimura (US 2003/0052324) and further in view of Kumatani (US 2002/0149119 A1).

Regarding claims 5, 6, 7, Yonezawa in view of Kimura discloses limitations in claims 1, 2 above and

- Jachimowicz et al in view of Kimura does not explicitly disclose the integrated circuit, the light emitting element and the light receiving element are attached to a substrate with an adhesive agent.
- However, Kumatani discloses the integrated circuit 5 (Fig. 1, Para. 34), the light emitting element 6 (Fig. 1, Para. 34) and the light receiving element 4 (Fig. 1, Para. 34) are attached to a substrate 8 (Fig. 1, Para. 34) with an adhesive agent (Para. 34). Kumatani teaches the above modification is used to obtain miniaturizing of the semiconductor device (Para. 26). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Yonezawa in view of Kimura's structure with

Kumatani's structure as suggested above to obtain miniaturizing of the semiconductor device (Para. 26).

Regarding claims 13-15, Yonezawa in view of Kimura and Kumatani discloses all limitations above in claims 1, 2, 5.

Claims 4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonezawa et al (Yonezawa, US 2003/0032213 A1), Kimura (US 2003/0052324) A1 in view of Nishi et al (US 6,590,633 B1).

Regarding claims 4, 12, Yonezawa modified by Kimura discloses some limitations in claims 1, 2 above and Yonezawa modified by Kimura further discloses the integrated circuit comprising a connection terminal and, a rectification circuit (Kimura, Fig. 14B, element "AMPLIFICATION ELEMENT") configured to rectify an alternating voltage generated by an antenna 2708 (Fig. 13G, Para. 190), a power supply circuit (Kimura, Fig. 14B, element VBi, Para. 22) configured to generate a power supply voltage (Kimura, Fig. 14B) by using a voltage outputted from the rectification circuit (Kimura, Fig. 14B). However, Kimura does not disclose a demodulation circuit and a logic circuit.

- However, Nishi et al disclose a demodulation circuit (col. 12, line 27) and a logic circuit (col. 12, line 20). Nishi teaches a demodulation circuit and logic circuit are used to management and control of the charging state and

the management and control of the communication port (col. 12, lines 22-24). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Yonezawa in view of Kimura's structure with Nishi's structure including demodulation circuit and logic circuit to manage and control charging state and the communication port (col. 12, lines 22-24).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonezawa et al (Yonezawa, US 2003/0032213 A1), Kimura (US 2003/0052324) and further in view of Nishi et al (US 6,590,633 B1) and Kumatani (US 2002/0149119 A1).

Regarding claim 8, Yonezawa modified by Kimura and Kumatani discloses some structural limitations above in claims 4, 5 and Yonezawa further discloses the integrated circuit 421, the light emitting element 433 and the light receiving element 441 formed integrally (Fig, 25C, 23B).

Claims 9, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonezawa et al (Yonezawa, US 2003/0032213 A1), Kimura (US 2003/0052324), Kumatani (US 2002/0149119 A1) and further in view of Nakamura (US 2004/0152392 A1).

Regarding claims 9, 16, Yonezawa in view of Kimura and Kumatani discloses limitations above but does not disclose the substrate is a plastic substrate.

- However, Nakamura discloses the second substrate is a plastic substrate 315 (Fig. 3A, Para. 127). Nakamura teaches plastic substrate is used to emit light from the light emitting elements (Para. 28, lines 1-2). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Yonezawa in view of Kimura's structure with Nakamura's structure including plastic substrate to emit light from the light emitting elements (Para. 28, lines 1-2).

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-11, 13-16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 3/8/10 have been fully considered but they are not persuasive for claims 4, 12 because:

Applicant's argued that the cited references either in singularity or in combination do not teach or suggest the amended limitation "….configured to rectify an alternating voltage generated by an antenna, a power supply circuit configured to generate a power

supply voltage by using a voltage outputted from the rectification circuit…" However, Examiner respectfully submitted that Kimura clearly discloses in figures 13G and 14B as discussed above. Also, the claims language do not recite the arrangement of the amended elements such as a power supply circuit, rectification circuit etc. Yonezawa in view of Kimura and Nishi discloses all structural limitations.

- Therefore, when the semiconductor compound recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ